REMARKS

Claims 3 and 6-7 are amended, no additional claims are canceled in this response, and claim 38 is added. Claim 2 was canceled in a previous response. As a result, claims 1 and 3-38 are now pending in this application.

No new matter has been added through the amendments to claims 3 and 6-7. Claim 3 has merely been rewritten in independent form to include all of the elements recited in the base claim and any intervening claims from which claim 3 had depended. Claims 6 and 7 were amended merely to change the dependency of these claims from claim 1 to claim 3.

No new matter has been introduced through new claim 38. Support for new claim 38 may be found throughout the specification, for example but not limited to claim 3 as originally filed.

§102 Rejection of the Claims

Claim 1 was rejected under 35 U.S.C. § 102(a) as being anticipated by Siers et al. (U.S. 6,269,386). Applicant disagrees that Siers et al. is a § 102(a) prior art reference. Applicant believes that Siers et al. is characterized as a reference under 35 U.S.C. § 102(e), and thus believes that Applicant also has the right as provided under 37 C.F.R. 1.131 to swear behind Siers et al. Therefore, Applicant does not admit that Siers et al. is prior art and reserves the right, as provided for under 37 C.F.R. 1.131, to "swear behind" Siers et al. Applicant respectfully traverses the rejection of claim 1.

Siers et al. in FIG. 1 discloses a functional diagram for a Kogge-Stone adder. However, Applicant does not believe that the adder in Siers et al. teaches each of the elements included in claim 1, as arranged in claim 1.

For example, claim 1 includes "a first circuit having a plurality of carry-merge stages connected in a series, . . . including a final carry generated by a final stage of the series, a first carry generated by a first stage of the series and a second carry generated by one of the plurality of stages of the series located between the first and final stages of the series". Claim 1 further includes "a second circuit connected to the first circuit and having a plurality of stages, the second circuit connected to receive the final carry and the second carry. . ."

With respect to the first circuit, the Office Action relies on all of the P6 circuits in FIG. 1 of Siers et al. The circuits labeled as "P6" in FIG. 1 of Siers et al. include blocks 102, 104, 106, and 108. However, as noted above, the first circuit of claim 1 includes a plurality of carry-merge stages connected in series, including a first stage of the series, a final stage of the series, and a plurality of stages located between the first and the final stages. Thus, claim 1 recites at least four stages included in the first circuit.

Siers et al. fails to teach at least four stages included in "a first circuit having a plurality of carry-merge stages connected in a series, . . . including a final carry generated by a final stage of the series, a first carry generated by a first stage of the series and a second carry generated by one of the plurality of stages of the series located between the first and final stages of the series," as recited in claim 1. The Office Action on page 2 refers to "C_{out}^{i} in Figure 3 and col. 2 lines 32-47" as teaching a final stage of the series. However, Siers et al. at column 2, lines 33-37 states,

> As shown in FIG. 1, C generator 116 provides carry-out terms c_{out}^{i} for i=0, 1, . . . n. **FIG. 3 also illustrates C generator 116** and provides the Boolean expression for the carry-out terms as a function of the effective group generate and group propagate terms and the carry-in term C_{in} .

Thus, Siers et al. discloses that Fig. 3 illustrates a C generator 116, which, as noted above, is not part of the "P6" blocks 102, 103, 106, and 108 relied upon in the Office Action to disclose the first circuit of claim 1. Thus, C generator 116 is not part of the first circuit as relied upon by the Office Action. In contrast, on page 3 the Office Action states,

> a second circuit (e.g. 116 for generating carry) connected to the first circuit and having a plurality of stages (e.g. all P6s circuits).

Thus, the Office Action's reliance on C generator 116 as a stage in the first circuit is contradicted by the later reliance on block 116 as teaching the second circuit of claim 1. Since block 116 in FIG. 1 of Siers et al. cannot represent both a stage in the first circuit and also represent a second circuit as recited in claim 1, the Office Action fails to show how Siers et al. teaches each of the elements as discussed above and as recited in claim 1.

In another example of elements recited in claim 1 and not taught by Siers et al., claim 1 includes a "**plurality of stages** of the series located between the first and the final stages of the series." The Office Action on page 3 relies on "output of 108" as teaching these elements.

However, while Applicant does not admit that block 108 is a stage as recited in claim 1, Sires et al. at column 1, lines 41-45 states,

> PG generators 102, 104, 106, and 108 provide group generate and group propagate terms. PG generators 102, 104, and 106 constitutes a first stage (level) and may be operated in parallel, and PG generator 108 constitutes **a second stage (level).** (Emphasis added).

Thus, Sires et al. describes PG generator 108 as a second stage (level), and thus, PG generator 108 clearly fails to describe a "**plurality of stages** of the series located between the first and the final stages of the series," as recited in claim 1.

In another example of elements included in claim 1 and not taught by Siers et al., claim 1 recites,

> **a first circuit** having a plurality of carry-merge stages connected in a series, the first circuit adapted to generate a group of carries, the group of carries including **a final carry generated by a final stage of the series,** a first carry generated by a first stage of the series and **a second carry generated by one of the plurality of stages of the series located between the first and final stages** of the series;
>
> a second circuit connected to the first circuit and having a plurality of stages, **the second circuit connected to receive the final carry and the second carry** and adapted to produce a pair of conditional carry, the second circuit adapted to generate additional carries missing from the group of carries to provide one carry for every group of a predetermined number of bits of the two binary numbers. (Emphasis added).

Thus, the second circuit in claim 1 is connected to receive a final carry and a second carry from the first circuit, wherein the second carry is generated by one of the plurality of stages in the series of stages locate between the first and final stages in the first circuit. The Office Action on page 3 relies on "(e.g. 116 connects C_{in} and output 108)" as teaching these elements. However, there is no description in Siers et al. of C_{in} being generated from "one of the plurality of stages of the series located between the first and final stages of the series," as recited in claim 1. Further, there is no disclosure in Siers et al. that C_{in} is a final carry generated by a final stage of the series, as recited in claim 1.

In contrast, Siers et al. at column 2, lines 40-41 states, "This carry-in term may result from the sum of other bits not shown in FIG. 1." While Siers et al. is not necessarily limited by

this statement, Applicant's representatives fail to find in Siers et al. a teaching of "the second circuit connected to receive the final carry and the second carry," as recited in claim 1.

For at least the reasons stated above, Siers et al. fails to teach a first circuit element and a second circuit element as recited in claim 1, and so fails to teach each of the elements included in claim 1, as arranged in claim 1. Thus, claim 1 is not anticipated by Siers et al., and so Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claim 1.

New claim 38 depends from claim 1, and therefore includes all of the elements recited in claim 1. For reasons analogous to those stated above with respect to claim 1, claim 38 is also not anticipated by Siers et al.

Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of all claims pending in the application.

Allowable Subject Matter

Claims 3-7 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 3 has been rewritten in independent form, including all of the elements included in the base claim and any intervening claims. Further, claims 4-7, including claims 6 and 7 as now amended, depend from claim 3. Applicant respectfully submits that claims 3-7 are in condition for allowance, and therefore respectfully requests notification that claims 3-7 are allowed.

Claims 8-37 were allowed. Applicant acknowledges the allowance of claims 8-37.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2132) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this ____ day of April, 2006.

ROBERT MADDEN Robert Madden

Name Signature